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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re PATENT APPLICATION of:

Applicant:	Seiji ANDOH
Serial No.:	09/376,063
Filed:	August 17, 1999
For:	PACKAGE STRUCTURE FOR A SEMICONDUCTOR DEVICE
Art Unit:	2835
Examiner:	M. Datskovsky
Attorney Ref:	OKI 226

APPEAL BRIEF

November 26,2001

Commissioner
for Patents
Washington, DC 20231

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed September 26, 2000.

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I. REAL PARTY IN INTEREST

Oki Electric Industry Co., Ltd.

II. RELATED APPEALS AND INTERFERENCES

NONE

III. STATUS OF CLAIMS

Claims 20, 22 and 24-28 are pending. Each of claims 20, 22 and 24-28 is under appeal.

IV. STATUS OF AMENDMENTS

Amendments have been filed on July 20, 2000, December 11, 2000, and June 5, 2001. All of these previously filed amendments have been entered. A fourth amendment is submitted with this Appeal Brief to place the application in a better condition for appeal, but as of the date hereof, it has not been considered or entered.

V. SUMMARY OF THE INVENTION

The present invention is directed to a package structure for a semiconductor device that has radiation solder bumps and connection solder bumps on the back surface for surface mounting the semiconductor device to a printed circuit board. The inventive semiconductor device, as recited in claim 20 and with reference to Figures 1 and 2 of the application, includes:

- a substrate 11a having a main surface and a back surface, the back surface having a central area, an intermediate area surrounding the central area, and a peripheral area surrounding the intermediate area;
- a semiconductor chip disposed on the main surface;
- a first bump unit 13 disposed in the central area of the back surface; and
- a second bump unit 14 disposed in the peripheral area of the back surface.

The first bump unit located in the central area of the substrate 11a includes a plurality of bumps that are spaced a

first distance apart from each other and radiate heat from the semiconductor device to the surface to which the device is mounted (see, for example, page 4, lines 20-21,. The second bump unit includes a plurality of bumps that are spaced a second distance apart from each other, the second distance being greater than the first distance between the bumps in first bump unit, and the second bump unit transmits signals to and from the semiconductor device to the printed circuit board to which it is mounted (see, for example, page 4, lines 21-26). In the first bump unit, bumps are spaced close together to achieve an improved coefficient of thermal conductivity between the semiconductor device and the surface on which it is mounted (see, for example, page 5, lines 16-22). Because the first unit of bumps carry no electrical signals, there is no concern that solder bridges may form between the closely spaced bumps of the first bump unit when the bumps are reflowed during the process of surface mounting the semiconductor device. On the other hand, the bumps of the second bump unit carry signals to and from the semiconductor device and are spaced further apart than those in the first bump unit so that short-circuits caused by solder bridges between the bumps of the second bump unit, formed during the mounting process, will not occur (see, for example, page 5, lines 10-15). For example, the diameter of the radiation bumps 13 and connection bumps 14 is 0.75 mm, the distance between the radiation bumps 13 is 1.00 mm and the distance between the connection bumps is 1.27 mm (page 5, lines 23-26). Preferably, the plurality of bumps included in the first bump unit and the second bump unit are spherical in shape.

In the present invention as claimed, the second distance (i.e., the distance between the connection bumps 14) is less than a third distance between the central area and the peripheral area on the back surface of the substrate 11a. In other words, as recited in claim 22, the width of the intermediate area between the central area and the peripheral area, is greater than the second distance.

To assure an adequate number individual signal connections for the semiconductor device, the plurality of bumps included in the second bump unit is preferably greater in quantity than the plurality of bumps included in the first bump unit (see, for example, page 4, lines 23-26).

In another aspect of the invention, as recited in claims 26 and 28, and with reference to Figures 3 and 4 of the application, the plurality of connection bumps 14 are spaced at a distance sufficient to assure that when heat treatment is applied causing the bumps of the first and second bump units to melt, the connection bumps 14 remain apart from each other and make individual connections to the connection pads 22 on the printed circuit board 20 (see, for example, page 5, lines 10-15). On the other hand, the radiation bumps 13 are sufficiently close to each other that upon application of the heat treatment to the device, they melt and become fused to each other as a unitary body 30 in contact with the radiation pads 21 on the printed circuit board 20 (see, for example, page 5, lines 16-22). As recited in claims 27 and 29, the bumps of the first and second bump units are preferably formed of solder (see, for example, page 4, lines 17-

19.

VII. BRIEF DESCRIPTION OF THE REFERENCES

The Barrow patent describes a ball grid array (BGA) integrated circuit package that has an outer two-dimensional array of solder balls and a center two-dimensional array of solder balls located on the bottom surface of the package substrate. The solder balls are typically reflowed to mount the package to a printed circuit board. Mounted on the opposite surface of the substrate is an integrated circuit that is electrically coupled to the solder balls by internal routing within the package. The outer array of solder balls is located outside the profile of the integrated circuit to reduce solder stresses induced by differential thermal expansion between the integrated circuit and a substrate. The center solder balls are typically routed directly to ground and power pads of the package to provide a direct electrical and thermal path from the integrated circuit to the printed circuit board.

The Nakamura patent describes a semiconductor device manufactured as a ball grid array (BGA) wherein shorting between a power supply terminal and a ground terminal in the array is prevented by interposing at least one solder ball functioning as a signal electrode between a solder ball functioning as a power supply electrode and a solder ball functioning as a ground electrode on the mounting surface of the package.

The Katchmar patent describes a surface mount area-array integrated circuit package consisting of a substrate, a

semiconductor die electrically and mechanically connected to the top surface of package substrate, an area-array of conductive surface mount terminations (e.g., solder balls) electrically and mechanically connected to the bottom of the package substrate and at least one adhesive mass. The adhesive mass is located on the bottom of the package substrate and replaces the conductive terminations in the area where the joint strain energy density is calculated to be the greatest. When mounted on a substrate, the adhesive mass adheres the package to substrate, achieving increased mechanical and electrical reliability.

VIII. THE REJECTION

In the final Official Action dated June 26, 2001, from which this Appeal is taken, claims 20, 22 and 24-29 stand rejected as obvious over Barrow, U.S. Patent No. 5,394,410, in view of Nakamura, U.S. Patent No. 6,225,702, and Katchmar, U.S. Patent No. 6,194,782. Further, claim 28 stands rejected under 35 U.S.C. §112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

IX. GROUPING OF CLAIMS

The invention is defined within groupings of claims (i) 20, 22 and 24-25, (ii) 26-27, and (iii) 28-29. Claims 22 and 24-25 stand or fall with their base claim 20, claim 27 stands or falls with its base claim 26, and claim 29 stands or falls with its base claim 28. Claims 20, 26 and 28 each recite features that form an

independent basis for allowance.

X. ARGUMENT

Appellants respectfully traverse the rejections based on the prior art applied against the claims now pending on appeal. As discussed below, it is respectfully submitted that the Examiner has not met the burden of proof in establishing that the appealed claims are obvious. It is further respectfully submitted that the rejections fail to provide the required factual basis or even a reasonable rational for the rejections, and fails to apply art that teaches or suggests the claimed invention.

1. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE

The initial burden of establishing a basis for denying patentability to a claimed invention rests upon the examiner. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Thorpe, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985); In re Piasecki, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984).

In rejecting claims under 35 U.S.C. 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). It also is incumbent upon the Examiner to provide a basis in fact and/or cogent technical reasoning to support the conclusion that one having ordinary skill in the art would have been motivated to combine references to arrive at a claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988). In so

doing, the Examiner is required to make the factual determinations set forth in Graham v. John Deere Co. of Kansas City, 383 U.S. 1, 148 USPQ 459 (1966), and to provide a reason why one having ordinary skill in the art would have been led to modify the prior art reference to arrive at the claimed invention. Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985). Such a reason must stem from some teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983). Inherency requires certainty, not speculation. In re Rijckaert, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); W. L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); In re Oelrich, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); In re Wilding, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). Objective evidence must be relied upon to defeat the patentability of the claimed invention. Ex parte Natale, 11 USPQ2d 1222 (BPAI 1988). Teaching away from the claimed invention by the prior art is a per se demonstration of lack of prima facie obviousness. In re Dow Chemical Co., 837 F.2d 469, 5 USPQ2d 1529 (Fed. Cir. 1988), In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), In re Nielson, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987)

Claims 20, 22 and 24-29 stand rejected as obvious over Barrow, U.S. Patent No. 5,894,410, in view of Nakamura, U.S. Patent No. 6,225,700, and Katchmar, U.S. Patent No. 6,194,782. As discussed below, it is respectfully submitted that the Examiner has not met the burden of proof in establishing the obviousness of the appealed claims.

The Examiner relies on Barrow for a teaching of most of the features of the semiconductor device claimed in the present application. Specifically, the Examiner points to Figures 3-5 of Barrow as disclosing a semiconductor device comprising: a substrate 12 having a main surface 14 and a back surface 16, wherein the back surface 16 has a central area 38, an intermediate area 42 surrounding the central area 38, and a peripheral area 36 surrounding the intermediate area 42; a semiconductor chip 18 formed on the main surface; a first bump unit formed of solder located in the central area of the back surface, wherein the first bump unit radiates heat from the semiconductor device (abstract, lines 12-15); a second bump unit formed of solder located in the peripheral area of the back surface, wherein the second bump unit transmits signals (column 3, lines 6-7), wherein the 2nd bump unit is greater in quantity of solder balls than the first bump unit, and the solder balls are spherical in shape.

The Examiner acknowledges, however, that Barrow does not teach a second distance between signal bumps being greater than a first distance between heat transferring bumps, the second distance being less than a third distance between the central

(heat transferring) area and the peripheral (signal) area; or the requirement that a distance between solder balls in the first bump (central-heat transferring) unit be small enough to allow the solder balls to melt and fuse to each other, creating a unitary body.

To overcome the above-acknowledged defects in Barrow, the Examiner argues that it is inherent when making a heat transfer path made of solder balls to locate them as close as possible, up to a solid layer of solder, in order to make the heat transfer path more efficient. But this argument is inconsistent with the teachings of Barrow. Barrow fails to disclose that the solder balls in the central area are any closer together than in the peripheral area, or otherwise make any distinction between the spacing of the solder balls in the different areas on the back of the substrate. In Barrow, while the center solder balls are used to improve thermal conductivity by providing a direct thermal path from the integrated circuit to the printed circuit board, they also serve as direct connections from the integrated circuit to the power and ground busses in the circuit board (Barrow column 3, lines 7-15). Thus, it is important to keep the solder balls in the central area of Barrow as far apart as those in the peripheral area, so as to avoid solder bridges that could short circuit the power and ground busses when the solder balls are reflowed to form a bond between the semiconductor device and the printed circuit board. The Examiner fails to provide any explanation of how the solder balls in the central of Barrow could be moved closer together without seriously compromising

their function as individual conductors for connecting the ground and power busses to the integrated circuit.

The Examiner points to Nakamura as disclosing a way to prevent shorting between a power supply and ground terminal in a ball grid array semiconductor device (Figures 1-7) by increasing the distance between solder balls (column 4, lines 10-18). The text referenced by the Examiner refers to figures 5-6 in which further isolation between power supply and ground terminals is achieved by removing some of the signal-carrying solder balls between them (compare figure 5 to figure 4). However, it is respectfully submitted that Nakamura fails to teach or suggest central and peripheral areas in which the spacing between solder balls is different, or that the spacing between solder balls in the peripheral area is less than the distance between the peripheral area and the central area, as required by independent claims 20, 26 and 28.

The principal teaching of Nakamura is that shorting between power supply and ground terminals in the grid array can be avoided by interposing signal-carrying solder balls between those connected to the power supply and ground buses (Nakamura column 2, lines 15-26). The Examiner fails to adequately explain how the teaching of Nakamura would be applied to the invention in Barrow. Barrow discloses that the array of solder balls in the peripheral area is coupled to the signal lines of the integrated circuit, while the array in the central area is coupled to the ground buses and power bus of the substrate (Barrow column 3, lines 6-9). Hence, the technique taught by Nakamura is not

applicable to the peripheral area of Barrow in which there are no power supply and ground connections. Nor would Nakamura seem applicable to the central area of Barrow, which does not have any signal connections. Nakamura teaches away from the spacing of solder balls closely together in the central area of Barrow to avoid shorting of the power supply and ground connections, rather than spacing them closely together to improve thermal conductivity between the integrated circuit and the surface to which it is mounted. Moreover, it is respectfully submitted that Nakamura entirely fails to teach or suggest solder ball spacing as a consideration in controlling the temperature of the integrated circuit.

The Examiner points to Katchmar as disclosing a way to create an efficient thermal conductive path in a ball grid array semiconductor device (Figures 1-6), by placing solder balls in closer proximity to each other (Figures 5-6) or by creating a unitary body 26 (Figure 4 and column 7, lines 35-52). What the figures and text referenced by the Examiner disclose is the use of closely-spaced solder balls 40 under the profile of the semiconductor device 18 in one embodiment, to a reduce stress on the solder balls 24 at the periphery of the semiconductor package that provide electrical connections to the semiconductor device. Unlike Barrow, Katchmar does not disclose that any of the central solder balls are used for electrical connections. Rather, Katchmar discusses solder balls in the central area only in the context of reducing stress and providing a thermal path between the semiconductor device and the printed circuit board

(Katchmar column 8, lines 30-39). The Examiner fails to provide any explanation of how this teaching of Katchmar might be combined with Barrow so as to preserve the independent power supply and ground connections that are in the central area of Barrow. As noted earlier, bringing the solder balls closer together increases the likelihood of creating short circuits between the power supply and ground connections in the central area of Barrow.

As noted above, the Examiner acknowledges that Barrow fails to teach the requirement, appearing in each of independent claims 20, 26 and 28, that the distance between solder bumps in the peripheral region (i.e., the second distance) be less than a third distance between the central (heat transferring) area and the peripheral (signal) area. The Examiner asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the second distance less than the third distance since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

The applicant disagrees with the assertion that the claimed relationship between the second distance and the third distance is merely the discovery of "the optimum or workable ranges" that involve "only routine skill in the art" that would render the claims obvious to one of ordinary skill. Rather, such features clearly patentably distinguished the independent claims over the teachings of the applied art references. Specifically, Barrow

discloses central and peripheral areas of solder bumps (see Figures 4-5), but does not disclose any requirement regarding the distance between them. Rather, the only general limitation is that the outer array of solder balls be located outside the dimensional profile of the integrated circuit to reduce stress induced by differential thermal expansion between integrated circuit and the substrate (Barrow column 1, lines 63-67). In Nakamura, no distinction is made between a central area and a peripheral area and hence, Nakamura does not discuss at all, any requirement regarding a distance between a central area and a peripheral area, and the relationship of that distance to the spacing between solder bumps in the peripheral area. Katchmar also lacks any clearly distinguishable central area and peripheral area, and fails to disclose any limitations regarding the spacing of the area containing the conductive surface mount terminations 14 from the adhesive mass 26 or central solder bumps 40 (Katchmar Figures 4-5). Thus, contrary to the Examiner's assertions, the applied prior art references lack any disclosure of a general limitation regarding the distance between central and peripheral areas of the semiconductor mounting package.

2. THE APPLIED REFERENCES FAIL TO SUGGEST THE CLAIMED INVENTION

In determining obviousness, the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed. Hartness Int'l, Inc. v. Simplimatic Eng'g Co., 819 F.2d 1100, 2 USPQ2d 1826 (Fed. Cir. 1987). It is impermissible to pick

and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. In re Wesslau, 353 F.2d 238, 147 USPQ 391 (CCPA 1951). Piecemeal reconstruction of prior art patents is improper, In re Kamm, 452 F.2d 1052, 172 USPQ 298 (CCPA 1972). The Examiner must give adequate consideration to the particular problems and solution addressed by the claimed invention. Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); In re Fothermel, 276 F.2d 393, 125 USPQ 328 (CCPA 1960).

The fact that the prior art could be modified so as to result in the combination defined by the claims does not make the modification obvious unless the prior art suggests the desirability of the modification. In re Deminski, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986). The test is what the combined teachings would have suggested to those of ordinary skill in the art. In re Keller, 642 F.2d 413, 208 USPQ 817 (CCPA 1981). Simplicity and hindsight are not proper criteria for resolving obviousness, In re Warner, supra. The proper approach to the issue of obviousness is whether the hypothetical person of ordinary skill in the art, familiar with the references, would have found it obvious to make a structure corresponding to what is claimed. In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983). Hindsight obviousness after the invention has been made is not the test. In re Carroll, 601 F.2d 1184, 202 USPQ 571 (CCPA 1979). The

reference, viewed by itself and not in retrospect, must suggest doing what applicant has done. In re Shaffer, 229 F2d 476, 108 USPQ 326 (CCPA 1956); In re Sokol, 523 F2d 1392, 187 USPQ 481 (CCPA 1975).

The issue is not whether it is within the skill of the artisan to make the proposed modification but, rather, whether a person of ordinary skill in the art, upon consideration of the references, would have found it obvious to do so. The fact that the prior art could be modified so as to result in the combination defined by the claims would not have made the modification obvious unless the prior art suggests the desirability of the modification. See In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984), In re Deminski, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986), In re Keller, supra. See In re Laskowski, F2d., 10 USPQ2d 1397 (CAFC 1989). References are not properly combinable or modifiable if their intended purpose or function is destroyed by the combination or modification. See In re Gordon, supra.

Obviousness does not require absolute predictability but a reasonable expectation of success is necessary. In re Clinton, 527 F.2d 1226, 188 USPQ 365 (CCPA 1976), Amgen, Inc. v. Chugai Pharmaceutical Co. Ltd., 927 f.2d 1200, 18 USPQ2d 1016 (Fed. Cir. 1991). A prior art suggestion for virtually endless experimentation is not a case of prima facie obviousness. In re Dow Chemical Co., 837 F.2d 469, 5 USPQ2d 1529 (Fed. Cir. 1988)

With respect to claims 20, 22 and 24-29 the Examiner asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made to make a second

distance between signal bumps being greater than a first distance between heat transferring bumps and big enough to prevent a shorting during installation as is done by Nakamura, and to make the first distance between solder balls in the first units small enough to allow the solder balls to melt and to fuse to each other creating a unitary body as is shown in Katchmar in the device by Barrow in order to enhance the dissipation of heat.

As noted above, the Examiner acknowledges that Barrow does not teach a second distance between signal bumps being greater than a first distance between heat transferring bumps, the second distance being less than a third distance between the central (heat transferring) area and the peripheral (signal) area; or the requirement that a distance between solder balls in the first bump (central-heat transferring) unit be small enough to allow the solder balls to melt and fuse to each other creating a unitary body.

It is respectfully submitted that one of ordinary skill in the art would not be motivated to combine Barrow and Nakamura as proposed by the Examiner. The principal teaching of Nakamura, as earlier noted, is the interposing of signal bumps between power supply and ground bumps to avoid direct short circuits between the latter. However, in Barrow, all of the signal bumps are in the peripheral area while all of power supply and ground bumps are in the central area (Barrow column 3, lines 6-9). Applying the teaching of Nakamura to Barrow might be accomplished by moving the power supply and ground connections to the peripheral area, but this could not be done without destroying some of the

principal purposes and benefits of the Barrow configuration, namely, lowering the self-inductance and reducing the switching noise of the integrated circuit (Barrow column 3, lines 13-15).

It is further respectfully submitted that one of ordinary skill in the art would not be motivated to combine Barrow, Nakamura and Katchmar, as proposed by the Examiner. Nakamura, like Barrow, discloses a uniform distance between solder bumps in all areas of the array, and hence would not suggest to one skilled in the art to reduce the spacing between the solder bumps in the central area. In this regard, the Examiner relies on Katchmar. But although Katchmar, as noted above, does discuss moving the solder bumps in the central area closer together, it does not readily suggest combination with Barrow, because it conflicts with Barrow's requirement for normal spacing in the central area to accommodate power supply and ground connections.

Claims 26 and 28 specifically require that the bumps of the first bump unit are sufficiently close to each other that upon application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body. Although Katchmar discloses in Figure 5 the use of solder balls arranged in closer proximity to each other under the die 18, it is respectfully submitted that Katchmar fails to teach or suggest that these solder balls are melted and fused together during heat treatment as claims 26 and 28 require. Rather, what Katchmar does disclose is the use of a solder mass 26 (Katchmar Figure 4) that bonds during the reflow process to both the solderable pad 32 on the bottom surface 16 of the package substrate 12 and the solderable

pad 34 on the top surface 30 of the substrate 28. Hence, it is respectfully submitted that claims 26 and 28 independently distinguish over the applied art references, whether taken individually or in combination.

It is respectfully submitted that the Examiner has, in hindsight, combined elements found in the prior art without demonstrating, as required, that a person of ordinary skill in the art, upon consideration of the references, would have found it obvious to do so in the manner defined by the claims of the present invention.

3. THE CLAIMS AS AMENDED ARE NOT INDEFINITE

After a final rejection or other final action, amendments may be made cancelling claims or complying with any requirement of form expressly set forth the previous Office action. Amendments presenting rejected claims in better form for consideration on appeal may be admitted. 37 C.F.R. §1.116(a).

Claim 28 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner asserts the claim comprises contradictory requirements. The Examiner point out that in lines 13-14 it is written that "...upon application of heat treatment to the device causing the bumps of the first and second bump units to melt, the bumps of the first bump unit remain apart from each other...", while in lines 16-18 it is written "...wherein the bumps of the first bump unit are

sufficiently close to each other that upon application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body."

It is clear from the specification of the present application that the quoted language from lines 13-14 should read "... upon application of heat treatment to the device causing the bumps on the first and second bump units to melt, the bumps of the second bump unit remain apart from each other..." As claim 28 recites in lines 9-10, "... a second bump unit formed in the peripheral area of the back surface for transmitting signals..." And as disclosed in the specification at page 5, lines 13-15 "... the connection solder bumps 14 are located with a predetermined pitch or distance so that the adjacent connection bumps 14 should not join each other by the heat treatment..." It is clear that the bumps of the second bump unit recited in claim 28 correspond to the connection solder bumps 14 disclosed in the specification and, accordingly, it is the bumps of the second bump unit that should not join each other as a result of the heat treatment.

To correct the language of claim 28 so that it agrees with the disclosure in the specification, an amendment is submitted with this Appeal Brief pursuant to 37 C.F.R. §1.116. Inasmuch as the amendment presents claim 28 in a better form for consideration on appeal, it is respectfully submitted that any section 112, second paragraph, rejection should be withdrawn and the amendment submitted herewith should be admitted.

CONCLUSION

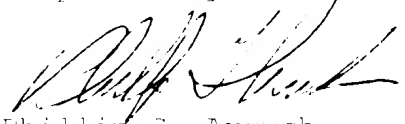
It is respectfully submitted that the Examiner has (i) failed to establish a prima facie case for the rejection, (ii) failed to apply art which teaches or suggests, the claimed invention, and (iii) has applied art in a manner inconsistent with its teachings.

Thus, it is respectfully submitted that the rejection of claims 20, 22 and 24-29 as obvious over Barrow, U.S. Patent No. 5,894,410, in view of Nakamura, U.S. Patent No. 6,225,702, and Katanmar, U.S. Patent No. 6,194,782, and the rejection of claim 28 under 35 U.S.C. §112, second paragraph, as indefinite, are improper.

In summary, it is submitted that the applied art does not provide any teaching, or suggestion within its teachings, which would lead to the features or advantages of the instant invention, and that the appealed claims patentably define over the art.

The rejection of claims 20, 22 and 24-29 under 35 U.S.C. §103(a), and of claim 28 under 35 USC §112, second paragraph, are in error and reversal is clearly in order and is courteously solicited.

Respectfully submitted,



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Appendix

APPENDIX

CLAIMS ON APPEAL

20. A semiconductor device, comprising:

a substrate having a main surface and a back surface,

wherein said back surface has a central area, an intermediate area surrounding said central area and a peripheral area surrounding said intermediate area;

a semiconductor chip disposed on said main surface;

a first bump unit disposed in said central area of said back surface,

wherein said first bump unit includes a plurality of bumps that are disposed a first distance apart from each other, and

wherein said first bump unit radiates heat from said semiconductor device; and

a second bump unit formed in said peripheral area of said back surface,

wherein said second bump unit includes a plurality of bumps that are disposed a second distance apart from each other, said second distance is greater than said first distance, and said second distance is less than a third distance between said central area and said peripheral area, and

wherein said second bump unit transmits signals.

22. The semiconductor device in accordance with Claim 20, wherein a width of said intermediate area of said back surface is greater than said second distance.

24. The semiconductor device in accordance with Claim 22, wherein said plurality of bumps included in said second bump unit is greater in quantity than said plurality of bumps included in said first bump unit.

25. The semiconductor device in accordance with Claim 24, wherein said plurality of bumps included in said first bump unit and said second bump unit are spherical in shape.

26. A semiconductor device, comprising:

a substrate having a main surface and a back surface, the back surface having a central area, an intermediate area surrounding the central area and a peripheral area surrounding the intermediate area;

a semiconductor chip disposed on the main surface;

a first bump unit disposed in the central area of the back surface to radiate heat from the semiconductor device, the first bump unit including a plurality of bumps disposed a first distance apart from each other; and

a second bump unit formed in the peripheral area of the back surface for transmitting signals, the second bump unit including a plurality of bumps disposed a second distance apart from each other, the second distance being greater than the first distance and less than a third distance between the central area and the peripheral area,

wherein the first and second distances are set such that

upon application of a heat treatment to the device, the bumps of the first bump unit melt so as to become connected and fuse to each other as a unitary body and the bumps of the second bump unit melt and remain apart from each other.

27. The semiconductor device according to claim 26, wherein the bumps of the first and second bump units are formed of solder.

28. A semiconductor device, comprising:

a substrate having a main surface and a back surface, the back surface having a central area, an intermediate area surrounding the central area and a peripheral area surrounding the intermediate area;

a semiconductor chip disposed in the main surface;

a first bump unit disposed in the central area of the back surface to radiate heat from the semiconductor device, the first bump unit including a plurality of bumps disposed a first distance apart from each other; and

a second bump unit formed in the peripheral area of the back surface for transmitting signals, the second bump unit including a plurality of bumps disposed a second distance apart from each other sufficient to assure that upon application of a heat treatment to the device causing the bumps of the first and second bump units to melt, the bumps of the first bump unit remain apart from each other, the second distance being greater than the first distance and less than a third distance between the central area

and the peripheral area,

wherein the bumps of the first bump unit are sufficiently close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body.

29. The semiconductor device according to claim 26, wherein the bumps of the first and second bump units are formed of solder.